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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,276	03/23/2004	Hideaki Fujiwara	57810-093	1866

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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
BRYANT, DELORIS S	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,276	FUJIWARA ET AL.	
	Examiner	Art Unit	
	Deloris Bryant	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 and 19-25 is/are rejected.

7)☒ Claim(s) 13-18 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/23/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1, 2 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunashima et al (US 6,376,888) in view of Hsu (US 5,677,214). Tsunashima teaches a gate insulator film (Fig. 11; 112) consisting of a high dielectric constant insulator film having a dielectric constant larger than 3.9 (col. 10, lns 59-60; Fig. 1E) and a gate electrode (Fig. 11; 113, 115) including a first metal layer (Fig. 11; 113) coming into contact with said gate insulator film (Fig. 11; 112) and having a work function controlled to have a Fermi level around the energy level of a band gap end of silicon constituting said source/drain regions (col. 11, lns 58-59). Tsunashima, however, fails to teach an elevated structure for the source/drain region. Hsu does teach a raised source/drain region (see Fig. 2-5). It would have been obvious to one of ordinary skill

in the art at the time of applicant's invention to incorporate Hsu's raised source/drain with Tsunashima's semiconductor device. One would have been motivated to so modify Tsunashima so that the susceptibility of the transistor to leakage current between junction areas is minimized (col. 1, lns 47-49).

Regarding claim 2, the prior art of Tsunashima and Hsu teach the limitations of claim 1 as described above. Furthermore, Tsunashima discloses said source/drain regions include n-type source/drain regions (Fig. 11) and said gate electrode (Fig. 11; 113, 115) includes said first metal layer (Fig. 11; 113) having said work function controlled to have a Fermi level around the energy level of the conduction band of silicon (col. 11, lns 58-59).

Regarding claim 6, the prior art of Tsunashima and Hsu teach the limitations of claim 1 as described above. Furthermore, Tsunashima discloses said gate insulator film (Fig. 11; 112) consisting of said high dielectric constant insulator film includes at least one film selected from a group consisting of an HfO_2 film, a ZrO_2 film and an HfAlO film (col. 10, lns 59-60; Fig. 1E).

Regarding claim 7-9 and 10, the prior art of Tsunashima and Hsu teach the limitations of claim 1 as described above. Furthermore, Tsunashima discloses a gate electrode includes a first metal layer having a controlled work function (col. 10, lns 66-67; col 11, lns 1-3) and a second metal layer, formed on the first metal layer, having a larger thickness than said first metal layer (See Fig. 11) (claim 7). Tsunashima also discloses a second metal layer having an uncontrolled work function (Fig. 11; 115) (claim 8) and that the second metal layer includes at least either a TaN layer or a TiN

layer (col. 16; lns 5-9) (claim 9). Tsunashima also teaches a first metal layer is formed in a U shape and that a second metal layer is formed to fill up a region enclosed with the U-shaped portion of the first metal layer (see Fig. 11) (claim 10).

3. Claims 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunashima et al (US 6,376,888) in view of Hsu (US 5,677,214) in further view of Cabral, Jr. et al (US 2005/0051854). The prior art of Tsunashima and Hsu teach the limitations as described above but fail to teach that the first metal layer includes an Hf layer. Cabral, Jr. does disclose that a first metal layer (Fig. 10; 700) of hafnium can be formed (claim 3). Cabral, Jr. also discloses a first metal layer (pg. 4; para. 0040) having said work function controlled to have a Fermi level around the energy level of the valence band of silicon (claim 4) that includes either a Ni layer or an Ir layer (pg. 4; para. 0040) (claim 5). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate Cabral, Jr's choice of material with Tsunashima's and Hsu. One would have been motivated to so modify both Tsunashima and Hsu to protect against dielectric breakdown without sacrificing transistor-switching performance (pg. 4; para. 0039).

4. Claims 11-12 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunashima et al (US 6,376,888) in view of Hsu (US 5,677,214) in further view of Zhang et al (US 5,563,426). The prior art of Tsunashima and Hsu teach the limitations as described above but fail to teach source/drain electrodes (claim

11) and a third metal layer (claim 12). Zhang, however, does teach a source/drain electrode (Fig. 7E; 715) which is formed by an aluminum film. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate Zhang's electrodes with the teaching of both Tsunashima and Hsu. One would have been motivated to so modify both Tsunashima and Hsu to employ a third metal layer that has a work function close to the conduction band of Si.

Regarding claim 21, Tsunashima teaches a gate insulator film (Fig. 11; 112) consisting of a high dielectric constant insulator film having a dielectric constant larger than 3.9 (col. 10, lns 59-60; Fig. 1E) and a gate electrode (Fig. 11; 113, 115) including a first metal layer (Fig. 11; 113) coming into contact with said gate insulator film (Fig. 11; 112) and having a work function controlled to have a Fermi level around the energy level of a band gap end of silicon constituting said source/drain regions (col. 11, lns 58-59). Tsunashima, however, fails to teach an elevated structure for the source/drain region. Hsu does teach a raised source/drain region (see Fig. 2-5). Tsunashima and Hsu fail to teach source/drain electrodes. Zhang, however, does teach a source/drain electrode (Fig. 7E; 715) which is formed by an aluminum film. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate Zhang's electrodes and Hsu's raised source/drain with Tsunashima's semiconductor device. One would have been motivated to so modify Tsunashima so that the susceptibility of the transistor to leakage current between junction areas is minimized (col. 1, lns 47-49) and to employ a third metal layer that has a work function close to the conduction band of Si.

Regarding claim 22, the prior art of Tsunashima, Hsu and Zhang teach the limitations of claim 21 as described above. Furthermore, Tsunashima discloses said source/drain regions include n-type source/drain regions (Fig. 11) and Zhang discloses said source/drain electrodes (Fig. 7E; 715) includes a metal layer (col. 16, line 50) having said work function controlled to have a Fermi level around the energy level of the conduction band of silicon.

5. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunashima et al (US 6,376,888) in view of Hsu (US 5,677,214) in further view of Horiuchi (US 2003/0034524). The prior art of Tsunashima and Hsu teach the limitations as described above in claim 1 but fàils to teach a silicon region where a silicon layer is formed on an insulator (claim 19) or an isolation insulator film formed on the outer sides of the source/drain region (claim 20). Horiuchi does disclose a silicon layer (Fig. 7; 3) formed on an insulator (Fig. 7; 2). Horiuchi also teaches an isolation layer on the outer sides of the source/drain region (Fig. 7; 4). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate Horiuchi's disclosure and teachings with the teaching of both Tsunashima and Hsu. One would have been motivated to so modify both Tsunashima and Hsu to provide superior isolation between adjacent devices and to improve performance due to reduced parasitic capacitances, which is what SOI devices are well known for in the art.

6. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunashima et al (US 6,376,888) in view of Hsu (US 5,677,214) and Horiuchi (US 2003/0034524) in further view of Cabral, Jr. et al (US 2005/0051854). The prior art of Tsunashima, Hsu and Horiuchi teach the limitations as described above but fail to teach that the metal layer includes an Hf layer (claim 23) or that the work function controlled to have a Fermi level around the energy level of the valence band of silicon (claim 24) that includes either a Ni layer or an Ir layer (claim 25). Cabral, Jr. does disclose that a first metal layer (Fig. 10; 700) of hafnium can be formed. Cabral, Jr. also discloses a metal layer (pg. 4; para. 0040) having said work function controlled to have a Fermi level around the energy level of the valence band of silicon that includes either a Ni layer or an Ir layer (pg. 4; para. 0040). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate Cabral, Jr's choice of material with Tsunashima, Hsu and Horiuchi. One would have been motivated to so modify Tsunashima, Hsu and Horiuchi to protect against dielectric breakdown without sacrificing transistor-switching performance (pg. 4; para. 0039).

Allowable Subject Matter

7. Claims 13-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deloris Bryant whose telephone number is (571) 272-8670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dsb

GEORGE ECKERT
PRIMARY EXAMINER